| FORM PTO-1449 (SUBSTITUTE)<br>U.S. DEPARTMENT OF COMMERCE<br>PATENT AND TRADEMARK OFFICE<br><br>INFORMATION DISCLOSURE STATEMENT BY APPLICANT<br>(37 CFR 1.98(b)) | Attorney Docket No.:<br>M&N-IT-197<br><br>Applicant<br>MARTIN EHLERT ET AL.<br><br>Filing Date<br>NOVEMBER 30, 2001 |
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| EXAMINER INITIALS | | PATENT NO. | DATE | PATENTEE | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|---|
| AV | A | 5,317,288 | 5/31/94 | Yung et al. | | | |
| AV | B | 5,614,855 | 3/25/97 | Lee et al. | | | |
| | C | | | | | | |
| | D | | | | | | |
| | E | | | | | | |
| | F | | | | | | |
| | G | | | | | | |
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FOREIGN PATENT DOCUMENT

| | | DOCUMENT NO. | DATE | COUNTRY | CLASS | SUB CLASS | TRANSL. YES | TRANSL. NO |
|---|---|---|---|---|---|---|---|---|
| AV | J | 19834416A1 | 02/04/99 | Germany | | | | X |
| | K | 19830571A1 | 01/13/00 | Germany | | | | X |
| | L | 0349715A2 | 01/10/90 | Europe | | | | X |
| | M | | | | | | | |
| | N | | | | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

| | | |
|---|---|---|
| AV | | Lee, Thomas H. et al.: "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE, Vol. 29, No. 12, December 1994, pp. 1491-1496 |
| AV | | Kim, C. et al.: "A 640 MB/s Bi-Directional Data Strobed, Double-Data-Rate SDRAM with a 40 mW DLL Circuit for a 256 MB Memory System", IEEE, February 6, 1998 |

| EXAMINER | DATE CONSIDERED |
|---|---|
| AV | 2/2/05 |

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.